CLAIMS

WHAT IS CLAIMED IS:

1. A microcontroller configurable as either an Alert Standard Format master or an Alert Standard Format slave, wherein the microcontroller is configured as either the Alert Standard Format master or the Alert Standard Format slave, wherein the microcontroller is further configured as an Advanced Configuration and Power Interface controller.

2. The microcontroller of claim 1, configured as the Alert Standard Format master.

3. The microcontroller of claim 2, wherein the microcontroller is coupled to an SMBus, and the microcontroller is further configured to receive Alert Standard Format status data from Alert Standard Format devices over the SMBus.

4. The microcontroller of claim 1, configured as the Alert Standard Format slave.

5. The microcontroller of claim 4, wherein the microcontroller is configured to receive status data from one or more Alert Standard Format devices, wherein the microcontroller is further configured to forward the status data from the one or more Alert Standard Format devices to the Alert Standard Format master.

6. The microcontroller of claim 1, further configured as an embedded 8051 microcontroller.

7. The microcontroller of claim 1, comprised in a bridge.

8. The microcontroller of claim 7, wherein the bridge is a south bridge.

9. An integrated circuit, comprising:

an internal bus; and

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus, wherein the microcontroller is configurable as either an Alert Standard Format (ASF) master or an ASF slave, wherein the microcontroller is configured as either the ASF master or the ASF slave, wherein the microcontroller is further configured as an Advanced Configuration and Power Interface (ACPI) controller.

10. The integrated circuit of claim 9, wherein the microcontroller is configured as the ASF master.

11. The integrated circuit of claim 10, wherein the microcontroller is coupled to an SMBus, wherein the microcontroller is further configured to receive ASF status data from one or more ASF devices over the SMBus.

12. The integrated circuit of claim 10, further comprising:

an Ethernet controller coupled to the internal bus, wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus.

13. The integrated circuit of claim 12, further comprising:

a plurality of buffers coupled between the microcontroller and the Ethernet controller for buffering the data.

14. The integrated circuit of claim 13, wherein the plurality of buffers are connected between the internal bus and the Ethernet controller.

15. The integrated circuit of claim 12, and wherein the Ethernet controller is configured to route Alert Standard Format messages to the microcontroller.

16. The integrated circuit of claim 12, further comprising:

a remote management and control protocol set command unit connected to the internal bus, wherein the remote management and control protocol set command unit is configured to execute remote management and control protocol commands received from an external management server through the Ethernet controller.

17. The integrated circuit of claim 9, wherein the microcontroller is configured as the ASF slave.

18. The integrated circuit of claim 17, wherein the microcontroller is configured to receive status data from one or more ASF devices, wherein the microcontroller is further configured to forward the status data from the one or more ASF devices to a remote ASF master.

19. The integrated circuit of claim 17, further comprising:

an Ethernet controller coupled to the internal bus, wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus.

20. The integrated circuit of claim 19, further comprising:

a plurality of buffers coupled between the microcontroller and the Ethernet controller for buffering the data.

21. The integrated circuit of claim 20, wherein the plurality of buffers are connected between the internal bus and the Ethernet controller.

22. The integrated circuit of claim 19, wherein the Ethernet controller is configured to route ASF messages to an external ASF master.

23. The integrated circuit of claim 9, wherein the microcontroller is further configured as an embedded 8051 microcontroller.

24. The integrated circuit of claim 9, wherein the integrated circuit is configured as a bridge, wherein the bridge further includes:

a first bus interface logic for coupling to a first external bus; and

a second bus interface logic for coupling to a second external bus.

25. The bridge of claim 24, wherein the bridge is configured as a south bridge.

26. The south bridge of claim 25, further comprising:

a plurality of south bridge registers; and

a register bridge connected to the internal bus, wherein the microcontroller is configured to read each of the plurality of south bridge registers through the register bride.

27. The integrated circuit of claim 9, further comprising:

a first ACPI embedded controller interface.

28. The integrated circuit of claim 27, further comprising:

a second ACPI embedded controller interface.

29. The integrated circuit of claim 28, further comprising:

a third ACPI embedded controller interface.

30. The integrated circuit of claim 9, further comprising:

an ASF status register.

31. An integrated circuit, comprising:

an internal bus;

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus, wherein the microcontroller is further configured as an Advanced Configuration and Power Interface (ACPI) controller; and

a plurality of ACPI embedded controller interfaces.

32. The integrated circuit of claim 31, wherein each of the plurality of ACPI embedded controller interfaces is configured as a private ACPI embedded controller interface.

33. The integrated circuit of claim 31, wherein the microcontroller is further configured as an embedded 8051 microcontroller.

34. The integrated circuit of claim 31, wherein the integrated circuit is configured as a bridge, wherein the bridge further includes:

a first bus interface logic for coupling to a first external bus; and

a second bus interface logic for coupling to a second external bus.

35. The bridge of claim 34, wherein the bridge is configured as a south bridge.

36. The south bridge of claim 35, further comprising:

a plurality of south bridge registers; and

a register bridge connected to the internal bus, wherein the microcontroller is configured to read each of the plurality of south bridge registers through the register bride.

37. An integrated circuit, comprising:

an internal bus;

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus, wherein the microcontroller is further configured as an Advanced Configuration and Power Interface (ACPI) controller;

an interrupt register configured to receive an entry from a processor, wherein an interrupt is generated to the microcontroller in response to the entry from the processor;

a data exchange register configured to receive one or more entries from the processor; and

one or more ACPI embedded controller interfaces.

38. The integrated circuit of claim 37, wherein the microcontroller is configured to write one or more entries in the data exchange register.

39. The integrated circuit of claim 37, wherein the microcontroller is configured to read the one or more entries in the data exchange register.

40. The integrated circuit of claim 37, wherein each of the one or more ACPI embedded controller interfaces is configured as a private ACPI embedded controller interface.

41. A computer system, comprising:

an external bus;

an integrated circuit, comprising:

an internal bus;

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus, wherein the microcontroller is configurable as either an Alert Standard Format (ASF) master or an ASF slave, wherein the microcontroller is configured as either the ASF master or the ASF slave, wherein the microcontroller is further configured as an Advanced Configuration and Power Interface (ACPI) controller; and

a bus interface logic connected to the external bus; and

a processor coupled to the external bus.

42. The computer system of claim 41, wherein the microcontroller is configured as the ASF master for the computer system.

43. The computer system of claim 42, further comprising:

an SMBus;

one or more ASF devices coupled to the SMBus; and

wherein the microcontroller is further configured to receive ASF status data from the one or more ASF devices over the SMBus.

44. The computer system of claim 42, further comprising:

an Ethernet controller coupled to the internal bus, wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus; and

wherein the processor is configured to communicate over a network using the Ethernet controller.

45. The computer system of claim 44, and wherein the Ethernet controller is configured to route Alert Standard Format messages to the microcontroller.

46. The computer system of claim 44, further comprising:

a remote management and control protocol set command unit connected to the internal bus, wherein the remote management and control protocol set command unit is configured to execute remote management and control protocol commands received from an external management server through the Ethernet controller.

47. The computer system of claim 41, wherein the microcontroller is configured as the ASF slave.

48. The computer system of claim 47, wherein the microcontroller is configured to receive status data from one or more ASF devices, wherein the microcontroller is further configured to forward the status data from the one or more ASF devices to a remote ASF master.

49. The computer system of claim 48, further comprising:

a network interface card coupled to the integrated circuit and to the processor, wherein the network interface card is configured as the Alert Standard Format master, and wherein the Ethernet controller is configured to route Alert Standard Format messages to the network interface card.

50. The computer system of claim 47, further comprising:

an Ethernet controller coupled to the internal bus, wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus.

51. A computer system, comprising:

an external bus;

an integrated circuit, comprising:

an internal bus;

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus, wherein the microcontroller is further configured as an Advanced Configuration and Power Interface (ACPI) controller;

a plurality of ACPI embedded controller interfaces; and

a bus interface logic connected to the external bus; and

a processor coupled to the external bus.

52. The computer system of claim 51, wherein each of the plurality of ACPI embedded controller interfaces is configured as a private ACPI embedded controller interface.

53. A computer system, comprising:

an external bus;

a processor coupled to the external bus; and

an integrated circuit, comprising:

an internal bus;

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus, wherein the microcontroller is further configured as an Advanced Configuration and Power Interface (ACPI) controller;

an interrupt register configured to receive an entry from the processor, wherein an interrupt is generated to the microcontroller in response to the entry from the processor;

a data exchange register configured to receive one or more entries from the processor;

one or more ACPI embedded controller interfaces; and

a bus interface logic connected to the external bus.

54. The computer system of claim 53, wherein each of the plurality of ACPI embedded controller interfaces is configured as a private ACPI embedded controller interface.

55. A method for operating a computer system, the method comprising:

receiving an Alert Standard Format message at a microcontroller in the Alert Standard Format south bridge;

receiving an ACPI event notification at the microcontroller in the Alert Standard Format south bridge; and

causing a system management interrupt to be generated using the microcontroller in the Alert Standard Format south bridge.

56. A method for operating a computer system, the method comprising:

receiving a first ACPI event notification at a first ACPI interface to a microcontroller in a south bridge; and

receiving a second ACPI event notification at a second ACPI interface to the microcontroller in the south bridge.

57. The method of claim 56, wherein receiving the second ACPI event notification at the second ACPI interface to the microcontroller in the south bridge comprises receiving the second ACPI event notification at the second ACPI interface to the microcontroller in the south bridge concurrently with receiving the first ACPI event notification at the first ACPI interface to the microcontroller in the south bridge.

58. The method of claim 56, further comprising:

receiving a third ACPI event notification at a third ACPI interface to the microcontroller in the south bridge.

59. The method of claim 58, wherein receiving the second ACPI event notification at the second ACPI interface to the microcontroller in the south bridge comprises receiving the second ACPI event notification at the second ACPI interface to the microcontroller in the south bridge concurrently with receiving the first ACPI event notification at the first ACPI interface to the microcontroller in the south bridge.

60. The method of claim 59, wherein receiving the third ACPI event notification at the third ACPI interface to the microcontroller in the south bridge comprises receiving the third ACPI event notification at the third ACPI interface to the microcontroller in the south bridge concurrently with receiving the first ACPI event notification at the first ACPI interface to the microcontroller in the south bridge.

61. The method of claim 57, further comprising:

receiving a fourth ACPI event notification at a fourth ACPI interface to the microcontroller in the south bridge.

62. The method of claim 57, further comprising:

causing a system management interrupt to be generated using the microcontroller in the south bridge.

63. A method for operating a computer system, the method comprising:

receiving an ACPI event notification at the microcontroller in the south bridge;

receiving one or more data entries in a data exchange register in the south bridge;

generating a microcontroller interrupt to the microcontroller in the south bridge; and

causing a system management interrupt to be generated using the microcontroller in the south bridge.

64. The method of claim 63, wherein generating the microcontroller interrupt to the microcontroller in the south bridge comprises generating the microcontroller interrupt to the microcontroller in the south bridge in response to receiving the one or more data entries in the data exchange register in the south bridge.

65. A computer readable medium encoded with instructions that, when executed by a computer system, performs a method for operating the computer system, the method comprising:

receiving an Alert Standard Format message at a microcontroller in the Alert Standard Format south bridge;

receiving an ACPI event notification at the microcontroller in the Alert Standard Format south bridge; and

causing a system management interrupt to be generated using the microcontroller in the Alert Standard Format south bridge.

66. A computer readable medium encoded with instructions that, when executed by a computer system, performs a method for operating the computer system, the method comprising:

receiving a first ACPI event notification at a first ACPI interface to a microcontroller in a south bridge; and

receiving a second ACPI event notification at a second ACPI interface to the microcontroller in the south bridge.

67. The computer readable medium of claim 66, wherein receiving the second ACPI event notification at the second ACPI interface to the microcontroller in the south bridge comprises receiving the second ACPI event notification at the second ACPI interface to the microcontroller in the south bridge concurrently with receiving the first ACPI event notification at the first ACPI interface to the microcontroller in the south bridge.

68. The computer readable medium of claim 66, the method further comprising:

receiving a third ACPI event notification at a third ACPI interface to the microcontroller in the south bridge.

69. The computer readable medium of claim 68, wherein receiving the second ACPI event notification at the second ACPI interface to the microcontroller in the south bridge comprises receiving the second ACPI event notification at the second ACPI interface to the microcontroller in the south bridge concurrently with receiving the first ACPI event notification at the first ACPI interface to the microcontroller in the south bridge.

70. The computer readable medium of claim 69, wherein receiving the third ACPI event notification at the third ACPI interface to the microcontroller in the south bridge comprises receiving the third ACPI event notification at the third ACPI interface to the microcontroller in the south bridge concurrently with receiving the first ACPI event notification at the first ACPI interface to the microcontroller in the south bridge.

71. The computer readable medium of claim 67, the method further comprising:

receiving a fourth ACPI event notification at a fourth ACPI interface to the microcontroller in the south bridge.

72. The computer readable medium of claim 66, the method further comprising:

causing a system management interrupt to be generated using the microcontroller in the south bridge.

73. A computer readable medium encoded with instructions that, when executed by a computer system, performs a method for operating the computer system, the method comprising:

receiving an ACPI event notification at the microcontroller in the south bridge;

receiving one or more data entries in a data exchange register in the south bridge;

generating a microcontroller interrupt to the microcontroller in the south bridge; and

causing a system management interrupt to be generated using the microcontroller in the south bridge.

74. The computer readable medium of claim 73, wherein generating the microcontroller interrupt to the microcontroller in the south bridge comprises generating the microcontroller interrupt to the microcontroller in the south bridge in response to receiving the one or more data entries in the data exchange register in the south bridge.

75. A south bridge, comprising:

controller means for receiving an Alert Standard Format message;

controller means for receiving an ACPI event notification; and

means for generating a system management interrupt.

76. A south bridge, comprising:

first interface means for receiving a first ACPI event notification; and

second interface means for receiving a second ACPI event notification.

77. The south bridge of claim 76, wherein the first interface means and the second interface means operate concurrently.

78. The south bridge of claim 76, further comprising:

third interface means for receiving a third ACPI event notification.

79. The south bridge of claim 78, wherein the first interface means and the third interface means operate concurrently.

80. The south bridge of claim 79, wherein the second interface means and the third interface means operate concurrently.

81. The south bridge of claim 76, further comprising:

fourth interface means for receiving a fourth ACPI event notification.

82. The south bridge of claim 76, further comprising:

means for generating a system management interrupt.

83. A south bridge, comprising:

controller means for receiving an ACPI event notification;

means for receiving one or more data entries in a data exchange register;

means for generating an interrupt to the controller means for receiving an ACPI event notification; and

means for generating a system management interrupt.

84. A bridge, comprising:

an internal bus configured to transfer data in the bridge; and

a microcontroller coupled to transmit data over the internal bus.

85. The bridge of claim 84, wherein the bridge is a south bridge.